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high-current, high-speed buffer

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The circuit shown in the diagram is intended for applications in which relatively large pulse-shaped signals are to be applied to a standard impedance of, say, 50 Ω. The parallel circuit of two high-speed buffers prevents overheating during periods of high loads and high drive.

The operational amplifiers used, Analog Devices' Type BUF104, have a bandwidth of 110 MHz and a very high slew rate: 3000 V µs^{-1}. The peak output current is 65 mA, which is not sufficient to provide 5 V into 50 Ω, but the parallel combination is able to. Connecting 100 Ω resistors, R_3 and R_4, in series with the outputs of the op amps gives an overall output impedance of 50 Ω.

Owing to the large bandwidth, effective decoupling is imperative, which is why its is advisable to use tantalum capacitors for C_3, C_4, C_7, and C_8 and ceramic ones for C_5, C_6, C_9, and C_{10}.

With output currents exceeding 50 mA, the pulse response may be enhanced by damping the self-inductance of the tantalum capacitors with the aid of series resistors of 1–4.7 Ω.

If the specified bandwidth of 110 MHz is to be attained, a central earth plane and SMT components must be used, since the parasitic self-inductance of standard components is too high. One of the prototypes constructed with standard components had a bandwidth of only 25 MHz. Also, with such a construction, the screening is less effective, so that at high frequencies positive feedback, and thus oscillations, may occur. This is the reason that there is an *RC* filter at the input of the op amps: R_1-C_1, and R_2-C_2 respectively, which limits the bandwidth to 80–90 MHz.

The circuit draws a quiescent current of ±15 mA. When the output signal is rectangular at a level of 10 V_{p-p}, into 50 Ω, the current drain rises to 60–65 mA.

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